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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,525	12/28/2001	Rajasekhar Pullela	1298/1F986-US2	7823

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,525	PULLELA ET AL.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,14-16 and 20* is/are rejected.

7)☐ Claim(s) *4,5,8-13 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10/8/04
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

NON-FINAL REJECTION

The rejections under 35 USC 112, second paragraph, and over Pullela (US 6,297,706) are withdrawn in view of the amendments to claim 14 and the arguments presented in the amendment.

The new prior art necessitated a new ground of rejection is below:

Claim Rejection

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2 and 6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,297,706 (706') in view of Voorman et al (US 5,103,117).

Claim 1 of the patent (706') discloses a latch circuit comprising:

- a trans-admittance circuit for receiving an input voltage and generating an output current; and

- a trans-impedance circuit for receiving the output current to output a voltage to the input of the trans-impedance circuit.

However, Claim 1 of the patent (706') does not disclose that the trans-impedance circuit is the active load, the trans-admittance circuit is clocked and the transmission line coupled between the trans-admittance circuit and the active load. Voorman et al teaches in Figures 1-2 a latch circuit comprising a clocked trans-admittance (T1, T2, T5, T5a, T6, T6A) clocked by clock signals (CLK, NCLK) and an active load (T3, T4, 6, 7) coupled to the clocked-admittance by unmarked transmission lines for controlling the latch circuit and improving decision accuracy, see lines 40-43, column 2. It would have been obvious to a person having skilled in the art at the time the invention was made to clock the trans-admittance circuit of the patent (706') and employ the active load circuit taught by the admitted prior art in the claimed circuit of patent (706') for the purpose of controlling the latch circuit and improving decision accuracy.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-7 and 20 are rejected under 35 USC 102 (b) as being anticipated by Voorman et al (US 5,103,117).

Voorman et al discloses in Figures 1-3 a latch circuit comprising:

- a clocked trans-admittance circuit (T1, T2, T5, T5A, T5, T6a) for receiving an input voltage (1, 2) and generating an output current at node 11 and at the collectors of the transistors (T5, T6);

- an active load (T3, T4, 6, 7) or a trans-impedance circuit for receiving the output current to produce output voltages (8, 9) coupled to the transistors (T5, T6) of the trans-impedance circuit as shown in Figure 1; wherein the active load being coupled to the clocked trans-admittance circuit by unmarked wiring lines;

- wherein said trans-admittance stage circuit comprising a first pair of transistors (T1, ,T2), a current source (4), a second pair of transistors (T5, T5A) and a third pair of transistors (T6, T6A) as recited in claim 3;

- wherein at least one latch pair (T3, T4, T7, T8) in Figure 3 coupled to receive the output currents at nodes (11, 14) to produce output current to nodes (8, 9) as recited in claim 7; and.

- wherein the active load circuit (T3, T4, 6, 7) coupled to a positive supply voltage (VCC=10) as recited in claim 20.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-15, 16 and 18 are rejected under 35 USC 103 (a) as being unpatentable over Voorman et al (US 5,103,117) in view of Hong (US 5,606,490).

Voorman et al (US 5,103,117) discloses in Figures 1-3 a latch circuit with of the limitations of the based claims and stated above but does not disclose a second latch circuit independently coupled to the first latch. Hong teaches in Figure 2 a circuit comprising latch circuits (22a-22d) are cascaded to increase the delay time. It would have been obvious to a person having skill in the art at the time the invention was made to cascade the latch circuit of Voorman et al as suggested by Hong for the purpose of increasing the delay time since the latch circuit of Voorman et al is the delay means.

With regard to claim 16, since the latch circuit of Voorman et al is clocked by opposite phases of the clock signal (CLK, NCLK), obviously the cascaded latch circuits would be clocked by the clock signal (CLK, NCLK).

With regard to claim 18, the collectors of the transistors (T1, T2, T5, T6) in Figure 1 of Voorman lack a common coupling point because they are not connected together.

Allowable Subject Matter

Claims 4-5, 8-13 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The claims are allowed because the prior art of record does not show the base of the

first and second transistors are clocked on opposite phases of a clock signal as combined in claim 4, the at least one latch pair includes two combined trans-admittance and additional trans-impedance stages as combined in claim 8 and the transistors having collectors directly coupled to the input and the output of the first combined stage as combined in claim 9.

Response to Applicant's Arguments

The applicant's arguments over the Pullela reference is moot without traverse.

CONCLUSION

Any comments considered necessarily by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH T. LE
PRIMARY EXAMINER